ISMVL 2013

IEEE 43rd International Symposium on Multiple - Valued Logic

Final Program

Toyama International Conference Center, Toyama, Japan, May 21 - 24

May 21, Tuesday		
9:00	Post-binary ULSI Workshop Registration	
10:00	Post-binary ULSI Workshop	
17:00	ISMVL Registration	
18:00	ISMVL Welcome Reception (ULSI WS Poster Session)	
May 22, Wednesday		
8:15	ISMVL Registration	
8:45	Opening	
9:00	**[Invited Address I]** **Computational Medical and Health Care Technology** *Yutaka Hata (University of Hyogo, Japan) and Hiroshi Nakajima (Omron Co., Japan)*	
9:50	Break	
10:10	**[Session 1A: Medical and Health Care Engineering]** **Systems Health Care – Health Management Technology –** *Hiroshi Nakajima, Toshikazu Shiga and Yutaka Hata*	**[Session 1B: Reversible Circuits]** **Fault Ordering for Automatic Test PatternGeneration of Reversible Circuits** *Robert Wille, Hongyan Zhang and Rolf Drechsler*
10:35	**Wearable Human Activity Recognition by Electrocardiograph and Accelerometer** *Tatsuhiro Fujimoto, Hiroshi Nakajima, Naoki Tsuchiya, Hideya Marukawa, Kei Kuramoto, Syoji Kobashi and Yutaka Hata*	**Synthesis of Reversible CircuitsBased on Exclusive Or Sums** *Ben Schaeffer, Linh Tran, Addison Gronquist, Marek Perkowski and Pawel Kerntopf*
11:00	**Gaze Estimation Using Electrooculogram Signals and Its Mathematical Modeling** *Mingmin Yan, Hiroki Tamura and Koichi Tanno*	**Multiple-Valued Reversible Benchmarks and Extensible Quantum Specification (XQS) format** *Maher Hawash, Martin Lukac, Michitaka Kameyama and Marek Perkowski*
11:25	**Fuzzy Damage Extraction Method for Ultrasonic Nondestructive Testing Images** *Koki Tsukuda, Tadahito Egawa, Kazuhiko Taniguchi, Kei Kuramoto, Syoji Kobashi and Yutaka Hata*	**Analysis and Improvement of Transformation-Based Reversible Logic Synthesis** *Chander Chandak, Anupam Chattopadhyay, Soumajit Majumder and Subhamoy Maitra*
11:50	Lunch (Symposium Committee)	

May 22, Wednesday (continued)		
13:00	**[Session 2A: Medical and Wellness Applications]** **A Fuzzy Human Detection for Security System Using Infrared Laser Camera** *Takahiro Takeda, Kei Kuramoto, Syoji Kobashi and Yutaka Hata*	**[Session 2B: Logic Design/Switching Theory I]** **Remarks on Applications of Shapes of Decision Diagrams in Classification of Multiple-Valued Logic Functions** *Stanislav Stanković, Radomir S. Stanković and Jaakko Astola*
13:25	**Mining Multi Human Locations Using Thermopile Array Sensors** *Masato Kuki, Hiroshi Nakajima, Naoki Tsuchiya, Kei Kuramoto, Syoji Kobashi and Yutaka Hata*	**A Machine to Evaluate Decomposed Multi-Terminal Multi-valued Decision Diagrams for Characteristic Functions** *Hiroki Nakahara, Tsutomu Sasao and Munehiro Matsuura*
13:50	**On Selection of Intraocular Power Formula Using Support Vector Machines and Genetic Algorithm** *Naotake Kamiura, Tomoya Fukuda, Ayumu Saitoh, Teijiro Isokawa, Nobuyuki Matsui and Hitoshi Tabuchi*	**An Application of Autocorrelation Functions to Find Linear Decompositions for Incompletely Specified Index Generation Functions** *Tsutomu Sasao*
14:15	**A Broken Line Classification Method of Mathematical Graphs for Automating Translation into Scalable Vector Graphic** *Noboru Takagi and Jianjun Chen*	**A Transfer Function Model for Ternary Switching Logic** *Mitchell A. Thornton*
14:40	**On Synthesis and Verification from Event Diagrams in a Robot Theatre Application** *Marek Perkowski, Aditya Bhutada, Martin Lukac and Mathias Sunardi*	**Spectral Response of Ternary Logic Netlists** *Mitchell A. Thornton and Theodore W. Manikas*
15:05	Break	
15:20	**[Session 3A: Clone Theory I]** **A Study on Essentially Minimal Clones** *Hajime Machida and Ivo G. Rosenberg*	**[Session 3B: Circuits I]** **Design and Evaluation of a Differential Switching Gate for Low-Voltage Applications** *Masanori Natsui, Kiyohiro Kashiuchi and Takahiro Hanyu*
15:45	**A Solution to a Problem of D. Lau: Complete Classification of Intervals in the Lattice of Partial Boolean Clones** *Miguel Couceiro, Lucien Haddad, Karsten Schölzel and Tamás Waldhauser*	**A Successive Approximation A/D Converter Using Generalized Non-Binary Algorithm** *Yuki Kurisu, Tatsuya Sasaki and Takao Waho*
16:10	**On the Clones Containing a Near-Unanimity Function** *Dmitriy Zhuk and Stanislav Moiseev*	**A Graph-Based Approach to Designing Parallel Multipliers over Galois Fields Based on Normal Basis Representations** *Kotaro Okamoto, Naofumi Homma and Takafumi Aoki*
16:35	**Intersections with Słupecki Partial Clones on a Finite Set** *Lucien Haddad and Karsten Schölzel*	**Low-Power Multiple-Valued Source-CoupledLogic Circuits Using Dual-Supply Voltages for a Reconfigurable VLSI** *Xu Bai and Michitaka Kameyama*
17:00	**Not Finitely Definable Partial Clones on a Finite Set** *Boris A. Romov*	**Dramatically Low-Transistor-Count High-Speed Ternary Adders** *Reza Faghih Mirzaee, Mohammad Hossein Moaiyeri, Mojtaba Maleknejad, Keivan Navi and Omid Hashemipour*

May 23, Thursday		
8:45	**[Invited Address II]** **The complexity of Łukasiewicz logic** *Martin Goldstern (Vienna University of Technology, Austria)*	
9:35	Break	
9:50	**[Session 4A: Clone Theory II]** **On Hyper Co-Clones** *Jelena Čolić, Hajime Machida and Jovanka Pantović*	**[Session 4B: Algebra and Logic I]** **Four Decades of Multi-Valued Logic: Lists of Highly Cited Papers** *Tsutomu Sasao*
10:15	**Clones of Partial Cofunctions** *Sebastian Kerkhoff and Friedrich Martin Schneider*	**Chaotic Time Series Prediction Using Neuro-Fuzzy Systems with Cluster-Based Tribes Optimization Algorithm** *Cheng-Hung Chen, Rong-Zuo Jhang and Yen-Yun Liao*
10:40	**Boolean Max-Co-Clones** *Andrei A. Bulatov*	**Join Operations on Commutative BCK-Algebras with Condition (S)** *Mayuka F. Kawaguchi, Kouta Minami and Michiro Kondo*
11:10	**[Special Talk]** **Local Energy Production for Local Consumption Using Micro Hydro Power** *Prof. Hiroyuki Uesaka (Toyama University of International Studies, Japan)*	
12:00	Excursion to Gokayama/Zuiryu-ji with lunch	
19:00	Banquet	
May 24, Friday		
8:45	**[Invited Address III]** **Highly Reliable Non-Volatile Logic Circuit Technology and Its Application** *Hiromitsu Kimura, Zhiyong Zhong, Yuta Mizuochi, Norihiro Kinouchi, Yoshinobu Ichida, and Yoshikazu Fujimori (Rohm Co., Ltd., Japan)*	
9:35	Break	
9:50	**[Session 5A: Algebra and Logic II]** **Tense Operators and Dynamic De Morgan Algebra** *Ivan Chajda and Jan Paseka*	**[Session 5B: Circuits II]** **Comparing Performance of a Multiple-Valued Time-Based Serial Data Link with Other Serial Links** *Mostafa Rashdan and James Haslett*
10:15	**On the Combinatorics of Tolerance Relations** *Dan A. Simovici*	**Lowering Error Floors in Stochastic Decoding of LDPC Codes Based on Wire-Delay Dependent Asynchronous Updating** *Naoya Onizawa, Warren Gross, Takahiro Hanyu and Vincent Gaudet*
10:40	**On Natural Eight-Valued Reasoning** *Norihiro Kamide*	**Expandable MVL Inverter Compatible with Standard CMOS Process and Its Application to MVL Hysteresis Comparator** *Arif Abdul Mannan, Koichi Tanno, Hiroki Tamura, Takako Toyama and Agung Darmawansyah*

May 24, Friday (continued)		
11:05	**Embedding-Based Methods for Trilattice Logic** *Norihiro Kamide*	**Accurate and High-Speed Asynchronous Network-on-Chip Simulation Using Physical Wire-Delay Information** *Takahiro Hanyu, Yuma Watanabe and Atsushi Matsumoto*
11:30	**On the Semigroup of Equational Classes of Finite Functions** *Jorge Almeida, Miguel Couceiro and Tamás Waldhauser*	**An Area-Efficient Multiple-Valued Reconfigurable VLSI Architecture Using an X-Net** *Xu Bai and Michitaka Kameyama*
11:55	Lunch (Executive Committee)	
13:20	**[Session 6A: Logic Design/Switching Theory II]** **Noise-Tolerant Model of a Ternary Inverter Based on Markov Random Field** *Golam Tangim, Svetlana Yanushkevich, Seiya Kasai and Vlad Shmerko*	**[Session 6B: Algebra and Reversible Circuits]** **Debugging of Reversible Circuits using πDDs** *Laura Tague, Mathias Soeken, Shin-ichi Minato and Rolf Drechsler*
13:45	**Minimization of the Number of Edges in an EVMDD by Variable Grouping for Fast Analysis of Multi-State Systems** *Shinobu Nagayama, Tsutomu Sasao and Jon T. Butler*	**Analysis of Reversible and Quantum Finite State Machines using Homing, Synchronizing and Distinguishing Input Sequences** *Martin Lukac, Michitaka Kameyama, Marek Perkowski and Pawel Kerntopf*
14:10	**Secure Key Storage Using State Machines** *Nan Li, Shohreh Sharif Mansouri and Elena Dubrova*	**Exact Template Matching Using Boolean Satisfiability** *Nabila Abdessaied, Mathias Soeken, Robert Wille and Rolf Drechsler*
14:35	**The Impact of Address Arithmetic on the GPU Implementation of Fast Algorithms for the Vilenkin-Chrestenson Transform** *Dušan Gajić and Radomir S. Stanković*	**Synthesis of Balanced Ternary Reversible Logic Circuit** *Bikromadittya Mondal, Pradyut Sarkar, Pranay Kumar Saha and Susanta Chakraborty*
15:00	**Solution of the Last Open Four-Colored Rectangle-free Grid – An Extremely Complex Multiple-Valued Problem** *Bernd Steinbach and Christian Posthoff*	**Contribution to the Study of Multiple-Valued Bent Functions** *Claudio Moraga, Milena Stanković, Radomir S. Stanković and Suzana Stojković*
15:25	**Ternary Logic Network Justification Using Transfer Matrices** *Mitchell A. Thornton and Jennifer L. Dworak*	**Alternative Proof of Mulholland's Theorem and New Solutions to Mulholland Inequality** *Milan Petrik, Mirko Navara and Peter Sarkoci*
15:50	Break	
16:00	Plenary Session:	
17:00	Closing:	
17:30 | 18:20	**[RM workshop invited address]** **Recent Topics on BDD/ZDD-Based Discrete Structure Manipulation** *S. Minato (Hokkaido University, Japan)*	
May 25, Saturday		
8:45	Reed-Muller Workshop	