43rd IEEE International Symposium on Multiple-Valued Logic
Toyama, Japan, May 22-24, 2013

CALL FOR PAPERS

The Multiple-Valued Logic Technical Committee of the IEEE Computer Society will hold its 43rd annual symposium in Toyama, Japan, on May 22-24, 2013. The event is sponsored by the IEEE Computer Society and Japan MVL Research Group. You are invited to submit an original paper, survey or tutorial paper on any subject in the area of multiple-valued logic, including but not limited to:

Algebra and Formal Aspects	Logic Design and Switching Theory
Automatic Reasoning	Test and Verification
Logic Programming	Spectral Techniques
Philosophical Aspects	Circuit/Device Implementation
Fuzzy Logic and Soft Computing	VLSI Architecture and Computing
Data Mining	System-on-Chip Technology
Machine Learning and Robotics	Nano Technology
Quantum Computing	Medical and Wellness Technology

Authors should submit papers by PDF or PS files using the software that will be available on the conference web site by **November 1, 2012**. Each manuscript should include a 50-100 word abstract, and should not exceed 6 pages in the 2-column IEEE Proceedings format.
Special issues of some journals are planned for selected ISMVL2013 papers.

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Authors will be notified about acceptance by **February 1, 2013**.
Photo-ready copies of accepted papers are due on **March 1, 2013**.
For submission details, visit: URL (http://mvl.jpn.org/ISMVL2013/)

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The symposium will be co-located with the International Workshop on Post-Binary ULSI Systems (May 21) and Reed-Muller 2013 Workshop (May 25).