Final Programme
3rd International Workshop on Applications of the
Reed-Muller Expansion in Circuit Design
(Reed-Muller 97)
In Cooperation with IFIP WG 10.5.

Place: Oxford University, Oxford, UK.
Date: September 19-20, 1997
just after ESSCIRC 97 (European Solid-State Circuits Conference)
Southampton, UK, September 16-18 .
This workshop focuses on the application of new techniques in the representation and realization of discrete functions. AND-EXOR based representations are often simpler than AND-OR based representations, and have other important properties. Decision diagrams are being extensively studied, and have offered powerful new techniques for verification and synthesis. The goal of the workshop is to bring together researchers in these and related fields to discuss new approaches and results. The first workshop was held in September 1993, in Hamburg, and the second in August 1995, in Tokyo.

Call for posters: As well as the refereed work listed below we are also making space available for the display of posters describing very recent work. If you'd like to take advantage of this, simply contact Frances Page at the address below with the title of your poster and a list of authors. Space will be allocated on a first come first served basis.

Enquiries :
Miss Frances Page
Oxford University Computing Laboratory
Wolfson Building, Parks Road
Oxford OX1 3QD, UK.
Tel: +44 1865 283505/273838
Fax: +44 1865 273839
Email: Frances.Page@comlab.ox.ac.uk

Further details are available on the website:
http://www.comlab.ox.ac.uk/oucl/users/jon.saul/ReedMuller97.html

****
FRIDAY 19 SEPTEMBER 1997
****
08.45-09.10 Registration
09.10-09.15 Welcome

09.15-09.40
Invited talk: Hybrid Spectral Transform Diagrams, Masahiro Fujita

09.40-10.05
Reordering Based Synthesis, Andreas Hett, Rolf Drechsler and Bernd Becker

10.05-10.30
ETDD-based Generation of Complex Terms for Incompletely Specified Boolean Functions, Gueesang Lee

****
10.30-11.30 Coffee and Posters
****

11.30-11.55
Minimized Generalized Partially Mixed Polarity Reed-Muller Expansion
M Marek-Sadowska, G Guner, T Krishnamurthy, S Gargeshwari and Ch Sharma

11.55-12.20
Exclusive-OR of Two Sum-of-Products Expressions: Simplification and an Upper Bound on the Number of Products, Debatosh Debnath and Tsutomu Sasao

12.20-12.45
New Fast Approach to Approximate ESOP Minimization for Incompletely

Specified Multi-Output Functions, Ning Song and Marek Perkowski

****
12.45-02.00 Buffet Lunch
****

02.00-02.25
Low Power Aspects of XOR based Circuit Design
Yibin Ye, Kaushik Roy and Rolf Drechsler

02.25-02.50
Lattice Diagrams Using Reed-Muller Logic
Marek Perkowski, Malgorzata Chrzanowska-Jeske and Yang Xu

02.50-03.15
Hardware Acceleration of Two-level ESOP Minimization Using CAMs
Jonathan Saul

****
03.15-04.00 Tea and Posters
****

04.00-04.25
Two Hierarchies of Generalized Kronecker Trees, Forms, Decision Diagrams and Regular Layouts, Marek Perkowski, Lech Jozwiak and Rolf Drechsler

04.25-04.50
Universal and Robust Testing of Stuck-Open Faults in Reed-Muller Canonical CMOS Circuits, D Das, S Chakraborty and B Bhattacharya

****
WORKSHOP DINNER
****

Day 1 Posters
****
In addition to posters relating to all the above papers the following will be displayed during Friday:

Non-Abelian Groups in Optimization of Decision Diagrams Representations of Discrete Functions, Radomir Stankovic

Reed-Muller Transform and Wavelets Theory: An Alternative Look at Reed-Muller Expansions, Radomir Stankovic and Yasushi Endow

Test Set Generation for Functional Decision Diagram Circuits using Genetic Algorithm, A Bystrov and A Almaini

A General Data Structure for XOR-Decomposition of Sets of Switching Functions, Bernd Steinbach and Christian Lang

Compact Testing of AND-EXOR Programmable Logic Arrays
Roustam Latypov

****
SATURDAY 29 SEPTEMBER 1997
****
09.15-09.40
Complexity Measures for AND-EXOR Expressions, Tsutomu Sasao

09.40-10.05
Minimizing Polynomial Implementation of Weakly Specified Logic Functions and Systems, Arkadij Zakrevskij

10.05-10.30
The Complexity of Symmetric Functions in the Polynomial Forms
Julia Manstivoda and Nikolay Peryazev

****

10.30-11.30 Coffee and Posters
****

11.30-11.55
Case Study: Manipulating EXOR-OBDDs by Means of Signatures
Christoph Meinel and Harald Sack

11.55-12.20
Compilation of Fast Manipulation Algorithms for K*BMDs
Stefan Horeth and Rolf Drechsler

12.20-12.45
Combinational Logic-Level Verification using Boolean Expression Diagrams
Henrik Hulgaard, Poul Williams and Henrik Andersen

****
12.45-02.00 , Buffet Lunch
****

02.00-02.25
A Heuristic Procedure for Finding AND-OR-XOR Expansions of Incompletely Specified Boolean Functions
Elena Dubrova, Michael Miller and Jon Muzio

02.25-02.50
A Canonical AND/EXOR Form that includes both the Generalized Reed-Muller Forms and Kronecker Reed-Muller Forms
Marek Perkowski, Lech Jozwiak and Rolf Drechsler

02.50-03.15
A Critique of Mixed Exclusive-/Inclusive-OR Logic Synthesis for the Xilinx XC6200 FPGA, Paul Metzgen and Jonathan Saul

****
03.15-04.00 Tea and Posters
****

04.00-04.25
A New Linearly Independent, Zhegalkin Galois Field Reed-Muller Logic
Karen Dill, Konika Ganguly, Robert Safranek and Marek Perkowski

04.25-04.55
Panel Session: Toward the future Reed-Muller Workshops
Panel Chair: T. Sasao

04.55-05.00 Closing

Day 2 Posters
****
Decision Diagrams for Discrete Functions Representations
Radomir Stankovic

On Self-dual Complements of Fixed Polarity Reed-Muller 2-forms
Ken Fok, Malgorzata Marek-Sadowska and Simone Boehringer

Evolutionary Minimization of Generalized Reed-Muller Forms
Karen Dill and Marek Perkowski

Decomposition of Logical Functions in Reed-Muller Logic
Elena Zaitseva and D Popel

Parallel and Distributed Algorithms for Minimization of Incompletely Specified Logic Functions in Reed-Muller Domain
Svetlana Yanushkevich, Grzegorz Holowinski, Vlad Shmerko and Elena Zaitseva
****