5th International Workshop on Applications of the Reed-Muller Expansion in Circuit Design

(Reed-Muller 01)

Mississippi State University
Starkville, MS, USA
August 10-11, 2001

PROGRAM

Thursday, August 9

1300 – 1700 On-site Registration – *Coskrey Auditorium, Memorial Hall on Campus*
1730 – 1900 Reception – *A. B. McKay Food Lab, Engineering Research Park*

Friday, August 10

0730 – 1130 On-site Registration – *Coskrey Auditorium, Memorial Hall on Campus*
(please note that all technical sessions will be in Coskrey Auditorium in Memorial Hall)

0830 – 0845 Opening Remarks

0845 – 1015 Session 1 - Decision Diagrams

Representation of Incompletely Specified Switching Functions Using Pseudo-Kronecker Decision Diagrams, *Munehiro Matsuura, Tsutomu Sasao*, p. 27

Improving XOR-Node Placement for ⊕-OBDDs, *Christoph Meinel, Harald Sack*, p. 51

Minimization of BDDs Using Linear Transformation of Variables, *A. V. Kolpakov, R. Kh. Latypov*, p. 57

1015 – 1045 Refreshment Break

1045 – 1215 Session 2 - Decomposition and Function Analysis

New Generalizations of Shannon Decomposition, *Pawel Kerntopf*, p. 109

A General Decomposition for Reversible Logic, *M. Perkowski, L. Jozwiak, P. Kerntopf, A. Mischenko, A. Al-Rabadi, A. Coppola, A. Buller, X. Song, M. Md. Mozammel Huq Azad Khan, S. Yanushkevich, V. Shmerko, M. Chrzanowska-Jeske*, p. 119

Boolean Representations of Binary Time Series, *D. Bochmann*, p. 139

1215 – 1330 Lunch

1330 – 1530 Session 3 - ESOP Minimization

SNF: A Special Normal Form for ESOPs, *Bernd Steinbach, Alan Mischenko*, p. 66

A Method to Find the Best Mixed Polarity Reed-Muller Expression Using Transeunt Triangle,

Gerhard W. Dueck, Dmitry Maslov, Jon T. Butler, Vlad P. Smerko, Svetlana N. Yanuskevich, p. 82

Algebra of MXOR/MXNOR Functions and their Usage in Boolean Function Minimization, *T. Raju Damarla, Wei Su*, p. 93

Fast Heuristic Minimization of Exclusive-Sums-of-Products, *Alan Mischenko, Marek Perkowski*, p. 242

1530 – 1600 Refreshment Break

1800 – 2030 Workshop Banquet (casual attire recommended) – *The Carregen House*

Saturday, August 11

0830 – 1000 Session 4 - Layout and Physical Design

Layout Driven Synthesis of Lattice Circuits, *Per Lindgren, Mikael Kerttu, Rolf Drechsler*, p. 159

Shannon and Davio Sets of New Lattice Structures for Logic Synthesis in Three-Dimensional Space, *Anas Al-Rabadi, Marek Perkowski*, p. 165

New Classes of Multi-valued Reversible Decompositions for Three-Dimensional Layout, *Anas Al-Rabadi, Marek Perkowski*, p. 185

1000 – 1030 Refreshment Break

1030 – 1200 Session 5 - Spectral Methods

Relating Arithmetic and Walsh Spectra for Verification by Implicit Error Modeling, *Katarzyna Radecka, Zeljko Zilic*, p. 205

Transformations Amongst the Walsh, Haar, Arithmetic and Reed-Muller Spectral Domains, *Mitch Thornton, D. Michael Miller, Rolf Drechsler*, p. 215

Families of New Multi-valued Reed-Muller-based Spectral Transforms, *Anas Al-Rabadi, Marek Perkowski*, 226

1200 – 1315 Lunch

1315 – 1415 Session 7 - Synthesis and Testing

An Algorithm for Detecting XOR-Type Logic, *Elena Dubrova, Tomas Bengtsson*, p. 271

Universal and Robust Testing of Stuck-Open Faults in GRM and EDOP Circuits, *Hafizur Rahaman, Debesh K. Das, Bhargab B. Bhattacharya*, p. 276

1415 – 1445 Refreshment Break

1445 – 1545 Session 8 – Quantum and Reversible Logic

Tutorial: Quantum and Reversible Logic, *Marek Perkowski*, (not in proceedings)

1545 – 1615 Roundtable Discussion and Plenary Session