6th International Symposium on

Representations and Methodology of Future Computing Technology

RM2003

March 10-11, 2003
Trier, Germany

Program :

Session 1: 10/03/2003, 9:15--10.45am

- *B. Steinbach, V. Yanchurin, M. Lukac*
  ON SNF Optimization: A functional Comparison of Methods (ps)
- *S. Stergios, G. Papakonstantinou*
  Towards a General Novel Exact ESOP Minimization Methodology (ps)
- *G. R. Pogosyan, I. G. Rosenberg*
  An Algorithm for Optimal Presentation of a Partial Boolean Function as a MOD2 sum of products (ps)

Session 2: 10/03/2003, 11:15--12.45pm

- *R. S. Stankovic, J. Astola*
  Application of Group Theory to Optimization Problems in Logic Design (ps)
- *M.H.A. Khan, M. A. Perkowski*
  Logic Synthesis with Cascades of New Reversible Gate Families (ps)
- *M. Miller G. Dueck*
  Spectral Techniques for Reversible Logic Synthesis (ps)

Session 3: 10/03/2003, 16:00--18.00pm

- *M. Ghasemzadeh, C. Meinel*
  BDDs, Horn Clauses and Resolution (ps)
- *T. Hirayama, T. Sato, Y. Nishitani*
  Minimizing AND-EXOR Expressions of Some Benchmark Functions (ps)
- *R. S. Stankovic, K. Egiazarian, M. Stankovic, J. Astola*
  Construction of Compact Word-Level Representations of Multiple-output Switching Functions by Wavelet Packets (ps)
- *A. Iseno, Y. Iguchi, T. Sasao*
  Fault Diagnosis for RAMS using WALSH Spectrum (ps)

Session 4 (Posters): 10/03/2003, 18:15--19:00pm

- *Y. Pottosin, E. Shestakov, V. Tomashev* (could not take place due to the absence of the authors)
  Multiplex Decomposition of Boolean Function of its Section Expansion (ps)
- *I. Jaganjac*
  Computing with Cellular Automata (ps)
- *A. Al-Rabadi* (could not take place due to the absence of the author)
  Reversible Logic Synthesis Using Iterativ Symmetry Indices Decomposition (ps)
- *G. Fyffe*
  Emulating XOR-BDDs with Conjunction Equivalence Diagrams (ps)

Session 5: 11/03/2003, 9:15--10.45am

- *J. Mathew, E. Dubrova*
  Totally Self-checking 1-out-of-n Checker with Applocation to Fault Tolerant Design (CD 2)
- *M. Homeister*
  Well-Structured Graph-Driven Parity-FBBDs (CD 2)
- *Ch. Meinel, H. Sack*

Variable Reordering von Parity-OBDDs (CD 2)

Session 6: 11/03/2003, 11:15--12.45pm

- *M. H.A. Khan, M. A. Perkowski*
  Multi-Output ESOP Synthesis with Cascades of New Reversible Gate Family (CD 2)
- *G. Dueck, D. Maslov*
  Reversible Function Synthesis with Minimum Garbage Outputs (CD 2)
- *D. Maslov, G. Dueck*
  Garbage in Reversible Designs of Multiple Output Functions (CD 2)

Session 7/8: 11/03/2003, 14:30--16.00pm

- *A. Al-Rabadi* (could not take place due to the absence of the author)
  New Multiple-Valued Quantum Logic Circuits (CD 2)
- *P. Kerntopf*
  Binary Decision Diagrams based on Single and Multiple Generalized Shannon Expansions (CD 2)
- *G. Yang, W.N.N. Hung, X. Song, M. A. Perkowski*
  Majority-Based Reversible Logic Gate (CD 2)
- *M. Perkowski, M. Lukac, M. Pivtoraiko, P. Kerntopf, M. Folgheraiter*
  A Hierarchical Approach to Computer Aided Design of Quantum Circuits (CD 2)

RM2003 Preliminary Program, Update 18 Mar. 2003, H. Sack