Call for Papers

— *Special Section on Multiple-Valued Logic and VLSI Computing* —

The IEICE Transactions on Information and Systems announces that it will publish a special section entitled "*Special Section on Multiple-Valued Logic and VLSI Computing* " in **September 2014.**

   Recent development of System-on-Chip (SoC) technology has been accelerated by device scaling which drives improved performance and power, high functionality and cost reduction. However, there occur unprecedented serious problems today at very small device feature sizes. To solve the problems, innovative new-concept VLSI computing technology such as multiple-valued VLSI computing is strongly expected to be developed. Also, logic design based on a multiple-valued concept, multiple-valued algebra and soft computing are expected to be effectively employed for the next-generation digital computing and artificial intelligent applications.   From this point of view, we have planned Special Section on Multiple-Valued Logic and VLSI Computing to be published in September, 2014. To discuss the same frontier area, the 43rd IEEE International Symposium on Multiple-Valued Logic (ISMVL2013) was held in May 2013 in Toyama, Japan. We solicit for submission of the papers on multiple-valued logic and VLSI computing, not limited to the presented papers in the ISMVL2013. We welcome demonstration of the recent development of novel and new-concept computing technology.

1. Scope
This special section aims at timely dissemination of research in these areas. Possible topics include, but are not limited to:
   Multiple-Valued Algebra and Logic, Fuzzy Logic, Soft Computing, Quantum Computing, Multiple-Valued Logic Design and Switching Theory, Test and Verification, Spectrum Technique, New-Concept VLSI Architecture, Multiple-Valued VLSI Computing, Nanodevice-Based Architecture.

2. Submission Instructions
   The standard number of pages is 8 for a PAPER and 2 for a LETTER. The maximum number of pages for the initial submission of a LETTER is 4. The page charges are considerably higher for extra pages. Manuscripts should be prepared according to the guideline in the "Information for Authors". The latest version is available at the web site, http://www.ieice.org/eng/shiori/mokuji_ess.html. The term for revising the manuscript after acknowledgement of conditional acceptance for this special section could be shorter than that for regular issues (60 days) because of the tight review schedule.

   This special section will accept only papers by electronic submission. Prospective authors are requested to follow carefully the submission process described below.
   1. Submit a manuscript and electronic source files (TeX/Word files, figures, authors' photos and biography) via the IEICE Web site https://review.ieice.org/regist_e.aspx **by November 29, 2013**. Authors should choose the [Special-LO] Multiple-Valued Logic and VLSI Computing as a "Type of Issue (Section)/Category of Transactions" on the online screen. Do not choose [Regular-ED].
   2. Send "Copyright Transfer and Page Charge Agreement" and "Confirmation Sheet of Manuscript Registration" by E-mail, FAX or postal mail to the following address (guest editor of the special section) by the above due date. We may withdraw the submission if these documents have not been received by the due date, even if the manuscript has been received by electronic submission. For additional guidelines on manuscript preparation, please visit: http://www.ieice.org/eng/shiori/mokuji_ess.html

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