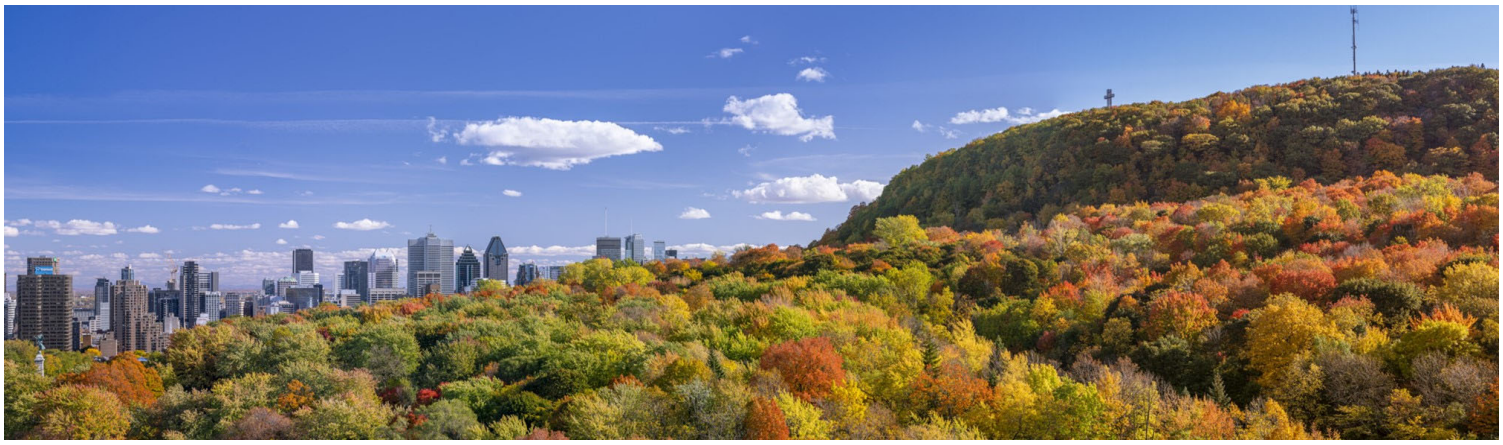
55th IEEE International Symposium on Multiple-Valued Logic

ISMVL 2025

June 5 – 6, 2025 Montreal, Quebec, Canada

Program



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June 4, Wednesday	
09:00	**Reed-Muller Workshop** @ Macdonald Engineering Building, Room 267
12:00	**Lunch**
13:20	**Workshop on Post-Binary ULSI Systems** @ Macdonald Engineering Building, Room 267
17:00	**ISMVL Welcome Reception & Poster Presentations from RM/ULSI** @ Faculty Club

June 5, Thursday		
08:00	**ISMVL Registration**	
08:45	**Opening** (Symposium Chair: *V. Gaudet* & *W. Gross*, Program Chair: *N. Onizawa* & *S. Nagayama*)	
09:00	**[Keynote Address I]** Chair: *H. Machida* **An Invitation to Surjective Polymorphisms** *Benoit Larose (LACIM, University of Quebec in Montreal / Champlain Regional College, Canada)*	
10:00	**Coffee Break**	
	[Session 1S] Chair: *N. Onizawa* **- Special Session on Spin-Edge Computing I -**	**[Session 1B]** Chair: *N. Kamide* **Non Classical Logics**
10:20	**Probabilistic Computing Utilizing Stochastic Spintronic Devices** *S. Fukami*	**Multi-Valued Models for Intuitionistic Logic** *A. Sakharov*
10:45	**Implementation of an MRAM-Based Edge AI Hardware with a Fine-Grained Power-Gating Technique** *T. Yoneda, Y. Takako, A. Tamakoshi, M. Natsui, D. Suzuki, and T. Hanyu*	**On Many-Valued Modal Probabilistic Logics** *O. Majer and I. Sedlar*
11:10	**Intelligent Power-Gating Technique with Quick Wake-Up/Sleep Functionality for Spintronics-Based Edge Computing Hardware** *F. Zhong, M. Natsui, and T. Hanyu*	**A Predicate Variant of Two-Layered Many-Valued Probability Logic** *L. Behounek*
11:35	**Enhanced Simulated Bifurcation for MIMO Detection** *R. Seah, T. Zhang, and W. J. Gross*	**A Complete Tableau Calculus for Signed MaxSAT** *J. Coll, C. M. Li, F. Manya, and E. Yangin*
12:00	**Lunch (Symposium & Executive Committee Meetings)**	
13:00	**[Keynote Address II]** Chair: *W. Gross* **Contribution of K. C. Smith in Applications of Multiple-Valued Logic** *Zeljko Zilic (McGill University, Canada)*	
	[Session 2] Chair: *Y. Yuminaka* **- KC Smith Special Session I -**	
13:35	**Memories of K. C. Smith: Analog Computing, Multiple-Valued Logic and Machine Learning** *V. Gaudet*	
13:50	**Hardware-Compatible U-Net for Low-Dose PET Reconstruction** *E.-K. Dao, K. Zukotynski, S. E. Black, and V. Gaudet*	
14:15	**Energy-Efficient Automated Seizure Detection in Wearable/Implantable BCIs: Motivations, Methods, and Example Implementation** *A. Dabbaghian and H. Kassiri*	
14:40	**Delta-Sigma Modulated Noise-Shaping Bitstreams for Multilayer Perceptron** *T. Waho, A. Koyama, and H. Hayashi*	
15:05	**Coffee Break**	
	[Session 3S] Chair: *T. Waho* **- Special Session on Spin-Edge Computing II -**	**[Session 3B]** Chair: *Y. Iijima* **Emerging Applications**
15:20	**Analog CMOS Spiking Neural Network for Time-Series Signal Recognition** *S. Sato, S. Moriya, M. Ishikawa, and H. Yamamoto*	**Binarization and Classification of RGB Images** *T. Nukenov, K. Abdiyeva, O. Keszocze, S. Nagayama, and M. Lukac*

15:45	**An FPGA-Based Rapid-Prototyping Platform for Spintronics-Based Edge-Computing Hardware** *D. Suzuki, A. Tamakoshi, T. Yoneda, M. Natsui, Y. Takako, and T. Hanyu*	**MUSIC Spectra using Cayley Graphs of Multiple-Valued Signals** *A. Sinha, D. Young, E. C. Larson, and M. A. Thornton*
16:10	**Simulation and Evaluation of Asynchronous Circuits in Extreme Edge Environments** *M. Imai*	**REBEL-6: A 32-Trit Balanced Ternary Instruction Set Architecture with R2R Compiler Pipeline for C** *S. Bos, V. Bodahl, O. C. Moholth, and H. Gundersen*
16:35	**Generating Hamiltonians with Known Minimum Energy Based on Ground-State Spin Logic for Probabilistic-Bit-Based Simulated Annealing** *N. Onizawa and T. Hanyu*	
17:00	**Free Time**	
18:00	**Banquet**	

June 6, Friday		
09:00	**[Keynote Address III]** Chair: *M. Miller* **Ground-State Logic Gates via Ising Hamiltonians** *Jacob Biamonte (Ecole de technologie sperieure – EST Montreal, Canada)*	
10:00	**Coffee Break**	
	[Session 4A] Chair: *G. Dueck* **Quantum Computing**	**[Session 4B]** Chair: *N. Homma* **Security**
10:20	**Reducing the Cost of Clifford+T Quantum Gates** *T. Ishioka, M. Lukac, and S. Nagayama*	**Hybrid Fingerprinting for Effective Detection of Cloned Neural Networks** *C. Aknesil, E. Dubrova, N. Lindskog, J. Sternby, and H. Englund*
10:45	**Realizing 4-Input Functions with the Minimum Toffoli Gate Count** *S. Yamashita, T. Horiyama, N. Yasuda, and T. Nakao*	**Decompressing Dilithium's Public Key with Fewer Signatures using Side Channel Analysis** *R. Wang, J. Gartner, and E. Dubrova*
11:10	**A Novel Data Representation Towards Efficient FPGA-Based Quantum Computer Simulation** *H. Hasegawa, M. Shimoda, H. Nakahara, and T. Miyoshi*	**Is Your Chip Leaking Secrets via RF Signals?** *Y. Ji, E. Dubrova, and R. Wang*
11:35	**Modeling and Simulation of Multiple-Valued and Nonlinear Quantum Photonic Components** *J. Ange, M. Tuller, J. M. Henderson, E. R. Henderson, B. A. Moores, D. L. MacFarlane, and M. A. Thornton*	**Solving AES-SAT using Side-Channel Hints: A Practical Assessment** *E. Dubrova*
12:00	**Lunch**	
	[Session 5A] Chair: *S. Yamashita* **Logic Design**	**[Session 5B]** Chair: *I. Sedlar* **Algebra, Clone, & Logic**
13:00	**Representation of Rotation Symmetric Multiple-Valued Functions Using Decision Diagrams** *S. Nagayama, T. Sasao, J. T. Butler, and M. Lukac*	**All Minimal Clones Generated by {0, 1}-Valued Majority Operations on a Five-Element Set** *M. Behrisch, E. Vargas-Garcia, and A. Wachtel*
13:25	**Linear Transformations for Iterative Reduction of Variables** *T. Sasao*	**On 2-Valued Majority Functions with Their Relation to Minimal Clones** *H. Machida*
13:50	**Normal Forms and Decompositions of Monotone Ternary Functions** *K. Schneider and N. Kercher*	**Foulis m-semilattices and their Modules** *M. Botur, J. Paseka, and M. Lekar*

14:15	**Additive Decomposition of Bent Functions** *C. Moraga, R. S. Stankovic, and M. Stankovic*	**Cut Elimination and Normalization in Intermediate Connexive Logics** *N. Kamide*
14:40	**Multi-Input MAGIC Synthesis and Verification for In-Memory Computing Design** *S. Nabipour, K. Datta, L. Weingarten, A. Kole, and R. Drechsler*	**Normalization Theorem for Extended Intuitionistic Belnap-Dunn Logic** *N. Kamide*
15:05	**Coffee Break**	
	[Session 6] Chair: *V. Gaudet* **- KC Smith Special Session II -**	
15:20	**On the Contributions to Multiple-Valued Logic by Prof. Kenneth C. Smith** *D. M. Miller*	
15:35	**Multi-Valued Data Transmission System using Mild Waveform Shaping Based on Multi-Dimensional Symbol Mapping** *Y. Iijima, A. Okada, and Y. Yuminaka*	
16:00	**Visualization of the Waveform Shaping Effect of Higher-Order FFEs using Multi-Valued Symbol Mapping** *Y. Yuminaka, R. Andachi, H. Zhang, and Y. Iijima*	
16:30	**Plenary Session & Closing**	

Brief Floor Map of Faculty Club (Main Level)