

55<sup>th</sup> IEEE International Symposium on Multiple-Valued Logic

# ISMVL 2025

June 5 – 6, 2025 Montreal, Quebec, Canada

## Program



Sponsored by:



## ISMVL 2025 Tentative Program (Overview)

Day 1 - Wednesday June 4	Day 2 - Thursday June 5	Day 3 - Friday June 6				
<b>9:00 - 12:00</b> Reed-Muller WS	<b>8:45 - 10:00</b> Opening & Invited Talk 1	<b>9:00 - 10:00</b> Invited Talk 3				
<b>12:00 - 1:20</b> Lunch	<b>10:00 - 10:20</b> Coffee Break	<b>10:00 - 10:20</b> Coffee Break				
<b>1:20 - 4:45</b> ULSI WS	<table border="1"> <tr> <td data-bbox="607 418 913 547"> <b>10:20 - 12:00</b>  <a href="#">Special Session on Spin-Edge Computing 1</a>                      (4 papers)                 </td> <td data-bbox="913 418 1216 547"> <b>10:20 - 12:00</b>  <a href="#">Logics</a>                      (4 papers)                 </td> </tr> </table>	<b>10:20 - 12:00</b> <a href="#">Special Session on Spin-Edge Computing 1</a> (4 papers)	<b>10:20 - 12:00</b> <a href="#">Logics</a> (4 papers)	<table border="1"> <tr> <td data-bbox="1243 418 1550 547"> <b>10:20 - 12:00</b>  <a href="#">Quantum Computing</a>                      (4 papers)                 </td> <td data-bbox="1550 418 1852 547"> <b>10:20 - 12:00</b>  <a href="#">Security</a>                      (4 papers)                 </td> </tr> </table>	<b>10:20 - 12:00</b> <a href="#">Quantum Computing</a> (4 papers)	<b>10:20 - 12:00</b> <a href="#">Security</a> (4 papers)
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<b>5:00 - 7:00</b> Welcome Reception (10 posters from RM/ULSI)	<b>12:00 - 1:00</b> Lunch	<b>12:00 - 1:00</b> Lunch				
	<b>1:00 - 1:35</b> <a href="#">Invited Talk 2</a>	<table border="1"> <tr> <td data-bbox="1243 616 1550 686"> <b>1:00 - 3:05</b>  <a href="#">Logic Design</a>                      (5 papers)                 </td> <td data-bbox="1550 616 1852 686"> <b>1:00 - 3:05</b>  <a href="#">Algebra &amp; Logic</a>                      (5 papers)                 </td> </tr> </table>	<b>1:00 - 3:05</b> <a href="#">Logic Design</a> (5 papers)	<b>1:00 - 3:05</b> <a href="#">Algebra &amp; Logic</a> (5 papers)		
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	<b>1:35 - 3:05</b> <a href="#">KC Smith Special Session 1</a> (4 papers)					
	<b>3:05 - 3:20</b> Coffee Break	<b>3:05 - 3:20</b> Coffee Break				
	<table border="1"> <tr> <td data-bbox="607 857 913 1031"> <b>3:20 - 5:00</b>  <a href="#">Special Session on Spin-Edge Computing 2</a>                      (4 papers)                 </td> <td data-bbox="913 857 1216 1031"> <b>3:20 - 5:00</b>  <a href="#">Applications</a>                      (4 papers)                 </td> </tr> </table>	<b>3:20 - 5:00</b> <a href="#">Special Session on Spin-Edge Computing 2</a> (4 papers)	<b>3:20 - 5:00</b> <a href="#">Applications</a> (4 papers)	<b>3:20 - 4:30</b> <a href="#">KC Smith Special Session 2</a> (3 papers)		
<b>3:20 - 5:00</b> <a href="#">Special Session on Spin-Edge Computing 2</a> (4 papers)	<b>3:20 - 5:00</b> <a href="#">Applications</a> (4 papers)					
	<b>5:00 - 6:00</b> Free Time	<b>4:30 - 5:00</b> TCMVL Plenary Session & Closing				
	<b>6:00 - 9:00</b> Banquet					

## ISMVL 2025 Tentative Program (Day 2 - Thursday June 5)

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### Special Session on Spin-Edge Computing 1

10:20	10:45	Implementation of an MRAM-Based Edge AI Hardware with a Fine-Grained Power-Gating Technique	Tomohiro Yoneda, Yasuhiro Takako, Akira Tamakoshi, Masanori Natsui, Daisuke Suzuki and Takahiro Hanyu
10:45	11:10	An FPGA-based rapid-prototyping platform for spintronics-based edge-computing hardware	Daisuke Suzuki, Tomohiro Yoneda, Yasuhiro Takako, Akira Tamakoshi, Masanori Natsui and Takahiro Hanyu
11:10	11:35	Probabilistic computing utilizing stochastic spintronic devices	Shunsuke Fukami
11:35	12:00	Analog CMOS Spiking Neural Network for Time-Series Signal Recognition	Shigeo Sato, Satoshi Moriya, Masaya Ishikawa and Hideaki Yamamoto

### Invited Talk 2

1:00	1:35	Contributions of K. C. Smith in Applications of MVL	Zeljko Zilic
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### KC Smith Special Session 1

1:35	1:50	<b>Opening to KC Smith Special Session:</b> Memories of K. C. Smith: Analog Computing, Multiple-Valued Logic and Machine Learning	Vincent Gaudet
1:50	2:15	Hardware-Compatible U-Net for Low-Dose PET Reconstruction	Eric-Khang Dao, Katherine Zukotynski, Sandra Black and Vincent Gaudet
2:15	2:40	Energy-Efficient Automated Seizure Detection in Wearable/Implantable BCIs: Motivations, Methods, and Example Implementation	Alireza Dabbaghian and Hossein Kassiri
2:40	3:05	Delta-sigma modulated noise-shaping bitstreams for multilayer perceptron	Takao Waho, Akihisa Koyama and Hitoshi Hayashi

### Special Session on Spin-Edge Computing 2

3:20	3:45	Intelligent Power-Gating Technique with Quick Wake-Up/Sleep Functionality for Spintronics-Based Edge Computing Hardware	Fangcen Zhong, Masanori Natsui and Takahiro Hanyu
3:45	4:10	Simulation and Evaluation of Asynchronous Circuits in Extreme Edge Environments	Masashi Imai
4:10	4:35	Enhanced Simulated Bifurcation for MIMO Detection	Ryan Seah and Warren J. Gross
4:35	5:00	Generating Hamiltonians with Known Minimum Energy Based on Ground-State Spin Logic for Probabilistic-Bit-Based Simulated Annealing	Naoya Onizawa and Takahiro Hanyu

### Logics

Multi-Valued Models for Intuitionistic Logic	Alexander Sakharov
On Many-Valued Modal Probabilistic Logics	Igor Sedlar and Ondrej Majer
A predicate variant of two-layered many-valued probability logic	Libor Behounek
A Complete Tableau Calculus for Signed MaxSAT	Jordi Coll, Chu-Min Li, Felip Manyà and Elifnaz Yangin

### Applications

Binarization and Classification of RGB Images	Kamila Abdiyeva, Tagir Nukenov, Oliver Keszocze, Shinobu Nagayama and Martin Lukac
{Multi-Modal CSNNs for Integrated Toxicity Detection Across Text, Audio, and Visual Modalities	Ismail El Sayad
MUSIC Spectra Using Cayley Graphs of Multiple-Valued Signals	Aviraj Sinha, Darrell Young, Eric Larson and Mitchell Thornton
REBEL-6: A 32-trit balanced ternary instruction set architecture with R2R compiler pipeline for C	Steven Bos, Vette Bodahl, Ole Christian Moholth and Henning Gundersen

**ISMVL 2025 Tentative Program (Day 3 - Friday June 6)**

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**Quantum Computing**

10:20	10:45	Reducing the Cost of Clifford-T Quantum Gates	Takehiro Ishioka, Martin Lukac and Shinobu Nagayama
10:45	11:10	Realizing 4-input Functions with the Minimum Toffoli Gate Count	Shigeru Yamashita, Takashi Horiyama, Norihito Yasuda and Tatsuya Nakao
11:10	11:35	A Novel Data Representation Towards Efficient FPGA-based Quantum Computer Simulation	Haruhiko Hasegawa, Masayuki Shimoda, Hiroki Nakahara and Takefumi Miyoshi
11:35	12:00	Modeling and Simulation of Multiple-Valued and Nonlinear Quantum Photonic Components	Joshua Ange, Mason Tuller, Jessie Henderson, Elena Henderson, Bradley Moores, Duncan MacFarlane and Mitchell Thornton

**Logic Design**

1:00	1:25	Representation of Rotation Symmetric Multiple-Valued Functions Using Decision Diagrams	Shinobu Nagayama, Tsutomu Sasao, Jon Butler and Martin Lukac
1:25	1:50	Linear Transformations for Iterative Reduction of Variables	Tsutomu Sasao
1:50	2:15	Normal Forms and Decompositions of Monotone Ternary Functions	Klaus Schneider and Nadine Kercher
2:15	2:40	Additive Decomposition of Bent Functions	Claudio Moraga, Radomir Stankovic and Milena Stankovic
2:40	3:05	Multi-Input MAGIC Synthesis and Verification for In-Memory Computing Design	Saeideh Nabipour, Kamalika Datta, Lennart Weingarten, Abhoy Kole and Rolf Drechsler

**KC Smith Special Session 2**

3:20	3:40	On the Contributions to Multiple-Valued Logic by Prof. Kenneth C. Smith	D. Michael Miller
3:40	4:05	Multi-Valued Data Transmission System Using Mild Waveform Shaping Based on Multi-Dimensional Symbol Mapping	Yosuke Iijima, Atsunori Okada and Yasushi Yuminaka
4:05	4:30	Visualization of the Waveform Shaping Effect of Higher-order FFEs Using Multi-valued Symbol Mapping	Yasushi Yuminaka, Ryou Andachi, Yosuke Iijima and Haohao Zhang

**Security**

Hybrid Fingerprinting for Effective Detection of Cloned Neural Networks	Can Aknesil, Elena Dubrova, Niklas Lindskog, Jakob Sternby and Håkan Englund
Decompressing Dilithium's Public Key with Fewer Signatures Using Side Channel Analysis	Ruize Wang, Joel Gärtner and Elena Dubrova
Is Your Chip Leaking Secrets via RF Signals?	Yanning Ji, Elena Dubrova and Ruize Wang
Solving AES-SAT Using Side-Channel Hints: A Practical Assessment	Elena Dubrova

**Algebra & Logic**

All minimal clones generated by $\{0, 1\}$ -valued majority operations on a five-element set	Mike Behrisch, Edith Vargas-García and Andreas Wachtel
On $\$2$ -valued majority functions with their relation to minimal clones	Hajime Machida
Foulis $m$ -semilattices and their modules	Michal Botur, Jan Paseka and Milan Lekár
Cut Elimination and Normalization in Intermediate Connexive Logics	Norihiro Kamide
Normalization Theorem for Extended Intuitionistic Belnap--Dunn Logic	Norihiro Kamide